1.5μA Ultra low Iq, 0.9V Startup, Ultra-High Efficiency Synchronous Boost

DESCRIPTION

ETA1161D is a high efficiency synchronous step-up converter with ultra-low quiescent current down to 1.5μA. It can deliver up to 7.5W of power from a low voltage source, i.e. 1.5A at 5V output (ETA1161D). It also features a true-shutoff function that disconnects the input from output, during shutdown and output short-circuit conditions. This eliminates the need for an external MOSFET and its control circuitry to disconnect the input from output and provides robust output overload protection.

A switching frequency of 1MHz minimizes solution footprint by allowing the use of tiny and low profile inductors and ceramic capacitors. An internal synchronous MOSFET provides highest efficiency and with a current mode control that is internally compensated, external parts count is reduced to minimal. With the ultra-low Iq feature, ETA1161 is ideal for solution that requires low standby power and compact board size such as IoT applications.

ETA1161 is housed in a CSP-6 and DFN2x2-6 package.

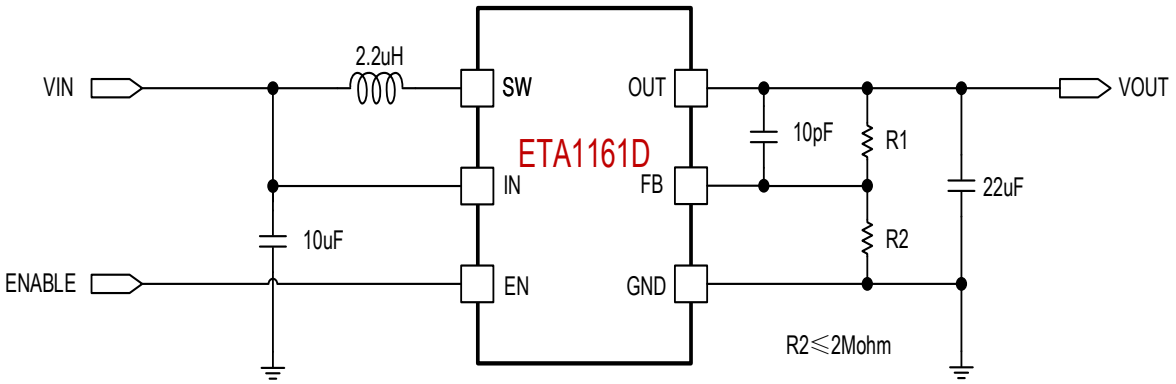
FEATURES

- Ultra-low IQ when No Switching:
  - 1.5uA for adjustable version
  - 1.55uA for fixed voltage version
- 0.9V Startup
- 5V/1.5A Output Capability at Vin=3V (ETA1161D)
- Output to Input Reversed Current Protection
- Up to 96% Efficiency
- Internal Synchronous Rectifier and Output Disconnect
- Short-circuit Protection
- Adjustable version and Fixed voltage version
- CSP-6 & DFN2x2-6 Package

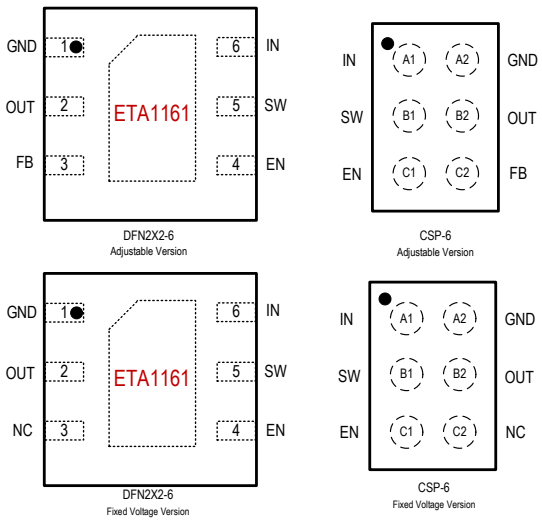
APPLICATIONS

- Tablet, MID
- Smart Phone
- Power Bank

TYPICAL APPLICATION



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN OUT, SW, FB, EN Voltage.....-0.3V to 6.5V
SW to ground current .....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range.....–55°C to 150°C
Thermal Resistance θ_{JA} θ_{JC}
CSP-6.....°C/W
DFN2x2-6.....80.....30.....°C/W
Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD CDM (Charged Device Mode) 1KV

ELECTRICAL CHARACTERISTICS

(V_{IN}=3.6V, V_{OUT} = 5V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current at OUT, adjustable version	V_{EN}=V_{IN}, No load, Not switching		1.5	2.5	μA
Quiescent Current at OUT, fixed voltage version	V_{EN}=V_{IN}, No load, Not switching		1.55	2.75	μA
Quiescent Current at IN, fixed 3.3V version	V_{EN}=V_{IN}=3.6V		3	4	uA
Shutdown Supply Current at IN	V_{EN} =GND		0.38		μA
IN Startup Voltage	I_{OUT}=1mA， Hysteresis=200mV		0.9		V
IN Operation Voltage	After Start-up	0.75		5.5	V
Input OVP			5.8V		V
Output OVP			10%VOUT		V
Output Voltage at 5V		4.85	5	5.15	V
Output Voltage at 3.3V		3.2	3.3	3.4	V
Feedback Voltage		0.98	1	1.02	V
Switching Frequency			1		MHz
NMOS Switch On Resistance	I_{SW}=100mA		140		mΩ
PMOS Switch On Resistance	I_{SW}=100mA		120		mΩ
SW Leakage Current	V_{OUT}=5.2V, V_{EN}=GND, V_{SW}=5.2V or V_{SW}= 0V			3	μA
NMOS Switch Current Limit	ETA1161A		1.2		A
	ETA1161B		1.8		A
	ETA1161C		2.5		A
	ETA1161D		3.1		A

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Linear PMOS Current Limit in Pass-Through Mode	ETA1161A		0.7		A
	ETA1161B		0.7		A
	ETA1161C		1.2		A
	ETA1161D		1.5		A
Start-up Current Limit			1.6		A
Short Circuit Hiccup time	ON		2		ms
	OFF		42		ms
EN Input Current	V_{EN}=5V or 0V	-1	0	1	μA
EN High Voltage	V_{OUT}=5V	1.2			V
EN low Voltage	V_{OUT}=5V			0.4	V
Thermal Shutdown	Rising, Hysteresis=25°C		150		°C

PIN DESCRIPTION

DFN2x2-6 PIN #	CSP-6 PIN #	NAME	DESCRIPTION
2	B2	OUT	Output pin. Bypass with a 4.7μF or larger ceramic capacitor closely between this pin and GND
1	A2	GND	Ground Pin
4	C1	EN	Enable pin for the IC. Drive this pin high to enable the part, low to disable.
6	A1	IN	Input Supply Voltage. Bypass with a 4.7μF ceramic capacitor to GND
3	C2	FB	Feedback Input. Add an external resistor divider from the OUT to FB and GND to set VOUT for adjustable output voltage. There is no FB pin for fixed voltage version. The pin is “Not Connected”.
5	B1	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.

APPLICATION INFORMATION

Loop Operation

ETA1161D is a high efficiency synchronous step-up converter with ultra-low quiescent current down to 1.5μA. It integrates a 140mΩ Low Side Main MOSFET and 120mΩ synchronous MOSFET. It uses a PWM current-mode control scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 3.2A. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

Ultra low current consumption at Light Load Operation

Traditionally, a fixed constant frequency PWM DC/DC regulator always switches even when the output load is small.

When energy is shuffling back and forth through the power MOSFETs, power is lost due to the finite RDSONs of the MOSFETs and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. ETA1161D employs a proprietary control scheme that improves efficiency in this situation by enabling the device into a power saving mode during light load and the no load quiescent current can be as low as 1.5μA.

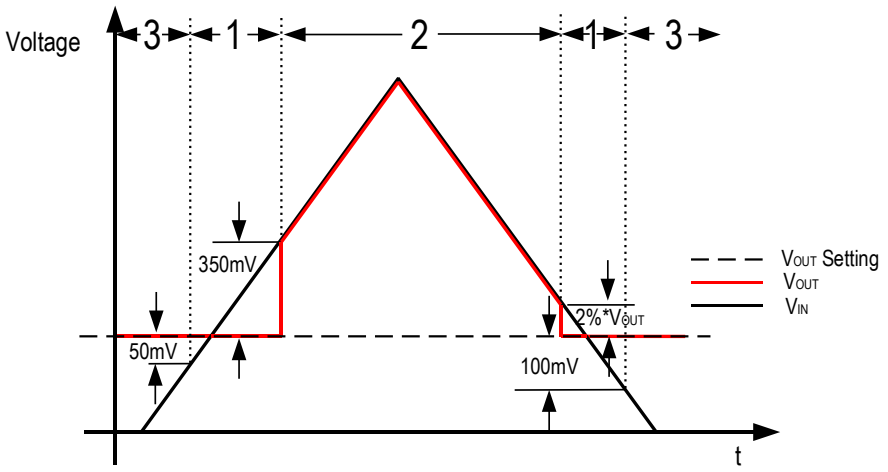
Down Mode Regulation and Pass-Through Operation

The ETA1161D features Down Mode and Pass-Through operation when input voltage is close to or higher than output voltage.

In the Down Mode, output voltage is regulated at target value even when VIN > VOUT. The control circuit changes the behavior of the rectifying PMOS by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the PMOS is increasing as high as to regulate the output voltage. The power loss also increases in this mode, which needs to be considered for thermal consideration.

In the Pass-Through operation, the boost converter stops switching. The rectifying PMOS constantly turns on and low side switch constantly turns off. The output voltage is the input voltage minus the voltage drop across the dc resistance (DCR) of the inductor and the on-resistance of the rectifying PMOS.

With VIN ramping up, the ETA1161D goes into Down Mode first when VIN > VOUT – 50mV. It stays in Down Mode until VIN > VOUT + 0.5 V and then goes automatically into Pass-Through operation. In the Pass-Through operation, output voltage follows input voltage. The ETA1611 exits Pass-Through Mode and goes back to Down Mode when VIN ramps down to 103% of the target output voltage. It stays in Down Mode until input voltage falls 100mV below the output voltage, returning to Boost operation.



Short-Circuit Protection

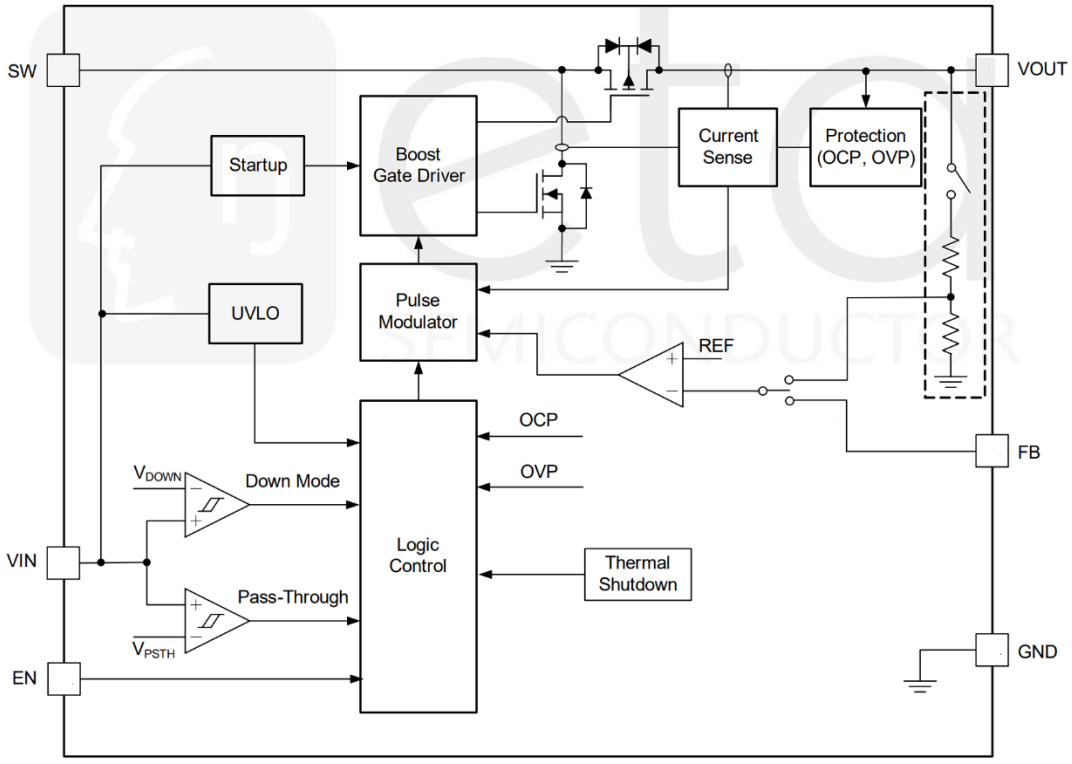
Unlike most step-up converters, the ETA1161D allows for short circuits on the output. In the event of a short circuit, the device first turns off the NMOS when the sensed current reaches the current limit. When OUT drops below IN, the device then enters a linear charge period with the current limited same as with the start-up period. In addition, the thermal shutdown circuits disable switching if the die temperature rises above 150°C.

Adjustable Output Voltage Setting with FB pin

By adding a resistor divider at FB pin (R1 and R2 as shown in the circuit below), ETA1161D can be set to any voltage level less than 5V at output node. The R2 is recommended to be 2Mohm or less, which will add about 0.5uA or more at output. The output voltage is set by following equation:

$$Vout=\frac{R1+R2}{R2}\times 1V$$

BLOCK DIAGRAM



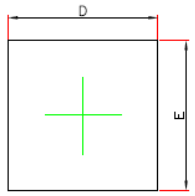
ORDERING INFORMATION

PART No.	Version	PACKAGE	TOP MARK	Pcs/Reel
ETA1161ACVG	Adjustable	CSP-6	1161A YWWL	3000
ETA1161AV33CVG	Fixed 3.3V Output	CSP-6	1161E YWWL	3000
ETA1161AV50CVG	Fixed 5.0V Output	CSP-6	1161F YWWL	3000
ETA1161BCVG	Adjustable	CSP-6	1161B YWWL	3000
ETA1161BV33CVG	Fixed 3.3V Output	CSP-6	1161G YWWL	3000
ETA1161BV50CVG	Fixed 5.0V Output	CSP-6	1161H YWWL	3000
ETA1161CCVG	Adjustable	CSP-6	1161C YWWL	3000
ETA1161CV33CVG	Fixed 3.3V Output	CSP-6	1161J YWWL	3000
ETA1161CV50CVG	Fixed 5.0V Output	CSP-6	1161K YWWL	3000
ETA1161DCVG	Adjustable	CSP-6	1161D YWWL	3000
ETA1161DV33CVG	Fixed 3.3V Output	CSP-6	1161L YWWL	3000
ETA1161DV50CVG	Fixed 5.0V Output	CSP-6	1161M YWWL	3000
ETA1161AD2G	Adjustable	DFN2x2-6	AiXX	3000
ETA1161AV33D2G	Fixed 3.3V Output	DFN2x2-6	UpXX	3000
ETA1161AV50D2G	Fixed 5.0V Output	DFN2x2-6	nBXX	3000
ETA1161BD2G	Adjustable	DFN2x2-6	AwXX	3000
ETA1161BV33D2G	Fixed 3.3V Output	DFN2x2-6	nLXX	3000
ETA1161BV50D2G	Fixed 5.0V Output	DFN2x2-6	nVXX	3000
ETA1161CD2G	Adjustable	DFN2x2-6	TiXX	3000
ETA1161CV33D2G	Fixed 3.3V Output	DFN2x2-6	N6XX	3000
ETA1161CV50D2G	Fixed 5.0V Output	DFN2x2-6	npXX	3000
ETA1161DD2G	Adjustable	DFN2x2-6	TwXX	3000
ETA1161DV33D2G	Fixed 3.3V Output	DFN2x2-6	yBXX	3000
ETA1161DV50D2G	Fixed 5.0V Output	DFN2x2-6	yVXX	3000

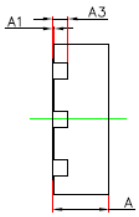
PACKAGE OUTLINE

Package: DFN2x2-6

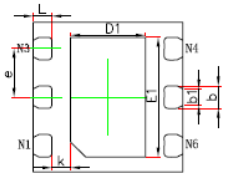
From assembly house 1：



TOP VIEW

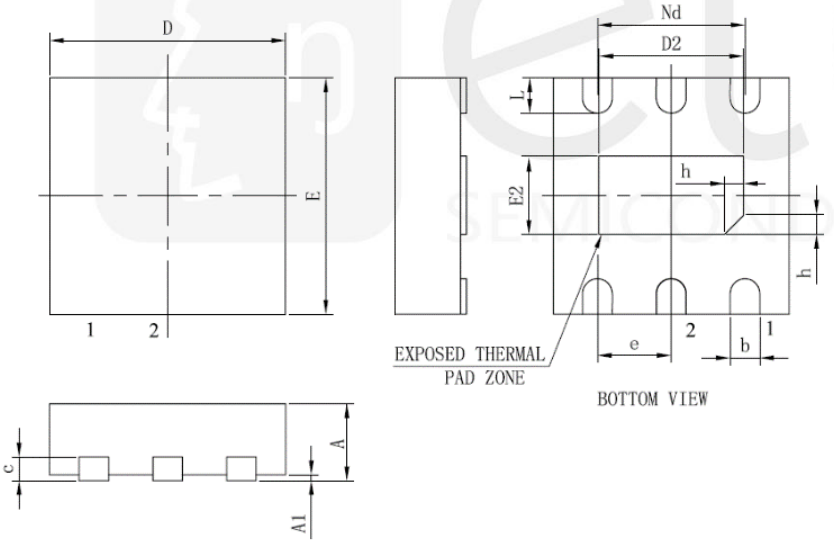


SIDE VIEW



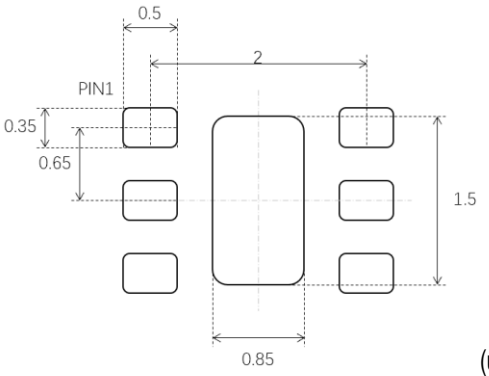
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
k	0.250 REF.		0.010REF.	
b	0.250	0.350	0.010	0.014
b1	0.220 REF.		0.009 REF.	
e	0.650BSC.		0.026BSC.	
L	0.174	0.326	0.007	0.013

From assembly house 2：



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	1.95	2.00	2.05
D2	1.00	1.23	1.45
e	0.65BSC		
Nd	1.30BSC		
E	1.95	2.00	2.05
E2	0.50	0.68	0.85
L	0.25	0.30	0.40
h	0.10	0.15	0.20

Recommend Land Pattern



(unit: Millimeter)

Package: CSP-6

Parameter	Nominal	Min	Max
	Millimeters		
Package Body Dimension X	0.840	0.820	0.860
Package Body Dimension Y	1.330	1.310	1.350
Package Height	0.590	0.560	0.620
Si thickness	0.355	0.3425	0.3675
Backside coating thickness	0.025	0.020	0.030
Solder Bump Height	0.210	0.190	0.230
Solder Bump Diameter	0.260	0.240	0.280
Total Ball Count per Die	6	/	/
Ball Pitch X axis	0.400	/	/
Ball Pitch Y axis	0.400	/	/