PIN NAME	PIN	Power Domain	Pull-Up	Pull-Down	Function0		Function1		Function2		Function3		Function4		Function5		Function6		Function7		Function8		Pin Config			Pin State			
					Function0	Type	Function1	Type	Function2	Type	Function3	Type	Function4	Type	Function5	Type	Function6	Type	Function7	Type	Function8	Type	Drive Strength	At Reset	After Reset	At Reset (H/L/Hiz)		After Reset (H/L/Hiz)	
I2S_BCK	4	VDD_EXT	20K/4.7K	40K	gpio_0	I/O	spi_flash1_clk	O	spi_2_clk	O	i2s2_bck	I/O	wcn_jtag_tck	I	uart_rxd_rf	I			debug_clk	O	wcn_ext_m_bb_senb	O	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
I2S_LRCK	5	VDD_EXT	20K/4.7K	40K	gpio_1	I/O	spi_flash1_cs	O	spi_2_ca_0	O	i2s2_lrck	I/O	wcn_jtag_tms	I	uart_txd_rf	O			debug_bus_0	O	wcn_ext_m_bb_sclk	O	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
I2S_DIN	6	VDD_EXT	20K/4.7K	40K	gpio_2	I/O	spi_flash1_sio_0	I/O	spi_2_dio_0	I/O	i2s2_sdat_i	I	wcn_jtag_tms	I	wcn_hst_txd	O			debug_bus_1	O			2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
I2S_DOUT	7	VDD_EXT	20K/4.7K	40K	gpio_3	I/O	spi_flash1_sio_1	I/O	spi_2_di_1	I	i2s2_sdat_o	O	wcn_jtag_tdi	I	wcn_hst_rxd	I			debug_bus_2	O			2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
MAIN_DTR	30	VDD_EXT	20K/4.7K	40K	gpio_4	I/O	spi_flash1_sio_2	I/O	spi_2_ce_1	O	pwl_out_0	O	wcn_jtag_tdo	I/O			i2c_m3_scl	I/O	debug_bus_3	O	wcn_ext_m_bb_sdo	O	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
MAIN_DCD	38	VDD_EXT	20K/4.7K	40K	gpio_5	I/O	spi_flash1_sio_3	I/O	pwm_pwl_out	O	lcd_fmark	I	wcn_uart_rts	O	wcn_uart_txd	O	i2c_m3_sda	I/O	debug_bus_4	O	wcn_ext_m_bb_sdi	I	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
PSM_EINT	96	V_PAD_1V8_RTC	20K/4.7K	40K	gpio_8	I/O	spi_1_ca_1	O	rfdig_gpio_8	I/O	lte_gpo_6	O			digrf_strobe_m_i	I	gpo_0	O	digrf_strobe_s_o	O			2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
AP_READY	19	V_PAD_1V8_RTC	20K/4.7K	40K	ap_jtag_tck	I	sdmmc2_cmd	I/O	spi_1_cs_0	O	zsp_jtag_tck	I	rfdig_jtag_tck	I	gpio_8	I/O							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SPI_CLK	26	V_PAD_1V8_RTC	20K/4.7K	40K	gpio_9	I/O	spi_1_clk	O	rfdig_gpio_9	I/O	lte_gpo_9	O	lte_spi_sdo	O			gpo_1	O					2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SPI_CS	25	V_PAD_1V8_RTC	20K/4.7K	40K	gpio_10	I/O	spi_1_ca_0	O	lte_spi_cs	O							gpo_2	O					2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
PSM_IND	1	V_PAD_1V8_RTC	20K/4.7K	40K	ap_jtag_tms	I	sdmmc2_data_1	I/O	spi_1_di_1	I	zsp_jtag_tms	I	rfdig_jtag_tms	I	gpio_10	I/O							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SPI_DOUT	64	V_PAD_1V8_RTC	20K/4.7K	40K	gpio_11	I/O	spi_1_dio_0	I/O	lte_spi_sclk	O							gpo_3	O					2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
NET_STATUS	21	V_PAD_1V8_RTC	20K/4.7K	40K	ap_jtag_tdi	I	sdmmc2_data_2	I/O	spi_1_cs_1	O	zsp_jtag_tdi	I	zsp_jtag_tdi	I	gpio_11	I/O							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SPI_DI	88	V_PAD_1V8_RTC	20K/4.7K	40K	gpio_12	I/O	spi_1_di_1	I	lte_spi_sdio	I/O							gpo_4	O					2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
STATUS	20	V_PAD_1V8_RTC	20K/4.7K	40K	ap_jtag_tdo	O	sdmmc2_data_3	I/O			zsp_jtag_tdo	O			gpio_12	I/O							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
MAIN_RI	39	VDD_EXT	20K/4.7K	40K	gpio_13	I/O	pwm_lpg_out	O															2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
I2C_SCL	40	VDD_EXT	20K/1.8K	40K	gpio_14	I/O	i2c_m2_scl	I/O															2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
I2C_SDA	41	VDD_EXT	20K/1.8K	40K	gpio_15	I/O	i2c_m2_sda	I/O															2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
MAIN_RTS	37	VDD_EXT	20K/4.7K	40K	gpio_18	I/O	uart_1_cts	I			zsp_uart_txd	O	wcn_uart_rxd	I	wcn_uart_cts	I							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
MAIN_CTS	36	VDD_EXT	20K/4.7K	40K	gpio_19	I/O	uart_1_rts	O	zsp_uart_cts	I	uart_3_txd	O	wcn_uart_txd	O	wcn_uart_rts	O							2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
AUX_RXD	28	VDD_EXT	20K/4.7K	40K	gpio_20	I/O	uart_2_rxd	I	uart_3_rxd	I	zsp_uart_rxd	I	uart_3_cts	I	zsp_uart_rts	O			debug_bus_12	O			2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
AUX_TXD	27	VDD_EXT	20K/4.7K	40K	gpio_21	I/O	uart_2_txd	O	uart_3_txd	O	zsp_uart_txd	O	uart_3_rts	O	zsp_uart_cts	I			debug_bus_13	O			2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
W_DISABLE	18	VDD_EXT	20K/4.7K	40K	gpio_22	I/O	uart_2_cts	I	uart_3_cts	I	zsp_uart_cts	I	uart_3_rxd	I	zsp_uart_txd	O	zsp_uart_cts	I	debug_bus_14	O	i2c_m3_scl	I/O	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SIM1_DET	42	VDD_EXT	20K/4.7K	40K	gpio_23	I/O	uart_2_rts	O	uart_3_rts	O	zsp_uart_rts	O	uart_3_txd	O	zsp_uart_rxd	I	uart_3_cts	I	debug_bus_15	O	i2c_m3_sda	I/O	2/4/6/8	ie=1, oe=0,wpd	ie=1, oe=0,wpd	INPUT	L	INPUT	L
SIM2_CLK	46	V_SIM2	20K/4.7K/1.8K	50K	sim_2_clk	O	gpo_5	O	gpio_29	I/O													2/4/6/8/10/12/15/17/20/25/28/30/32/34/37/39/42	ie=0, oe=1,wpd	ie=0, oe=1,wpd	OUPUT	L	OUPUT	L
SIM2_DAT	45	V_SIM2	20K/4.7K/1.8K	50K	sim_2_dio	I/O	gpo_6	O	gpio_30	I/O	uart_1_cts	I											2/4/6/8/10/12/15/17/20/25/28/30/32/34/37/39/42	ie=0, oe=1,wpu	ie=0, oe=1,wpu	OUPUT	H	OUPUT	H
SIM2_RST	44	V_SIM2	20K/4.7K/1.8K	50K	sim_2_rst	O	gpo_7	O	gpio_31	I/O	uart_1_rts	O											2/4/6/8/10/12/15/17/20/25/28/30/32/34/37/39/42	ie=0, oe=1,wpd	ie=0, oe=1,wpd	OUPUT	L	OUPUT	L